ABSTRACT:

An integrated circuit (100) has a plurality of inputs (110) and a plurality of outputs (120). In a test mode, a test arrangement including a plurality of logic gates (140) is coupled between the plurality of inputs (110) and the plurality of outputs (120). The logic gates from the plurality of logic gates (140) have a first input coupled to an input of the plurality of inputs (110) and a further input coupled to a fixed logic value source (150). The fixed logic value source (150) is used to define an identification code of the integrated circuit (100), which can be retrieved at the plurality of outputs (120) when an appropriate bit pattern is fed to the plurality of inputs (110).

Fig. 1